International Journal of Advance and Applied Research
www.ijaar.co.in
ISSN – 2347-7075 Impact Factor – 7.328
Peer Reviewed Bi-Monthly
Vol.10 No.3 January – February 2023

AN ANALYSIS ON THE THEORY OF VLSI MODELING TECHNIQUES

Mrs. Kamala Rasagana Tenneti[1] & Dr.Alok Agarwal[2]

[1]*Ph.D. Research Scholar, Department of Electronics & Communication Engineering, Shri. J.J.T. University, Rajasthan, India.*

[2]*Professor & Ph.D. Research Guide, Department of Electronics & Communication Engineering, Shri. J.J.T. University, Rajasthan, India.*

Corresponding Author - Mrs. Kamala Rasagana Tenneti

DOI - 10.5281/zenodo.7779913

Abstract:

Computerized circuits improve on the activity of semiconductors and permit gadgets to be worked as switches. Coming of vacuum tube tremendously affected the hardware business however a few obstructions like high power and 100 anode pressure. In the microelectronics business the development of semiconductor consumed not many watts. It turned into the establishment for lowenergy apparatuses. The reconciliation of various capabilities into a solitary chip and improvement of circuit execution have prompted a diminishing in the usefulness and a development of force for every unit region, which thusly has been supplemented by heat evacuation and cooling framework prerequisites. All through the VLSI climate, low power is the greatest issue for them.

Keywords: Digital circuits, transistors, vacuum tube, VLSI

Introduction:

In this day and age of the hardware business low power has arisen as a fundamental subject. The region, power utilization and speed are the fundamental worries for VLSI originators. Dissemination of force has turned into a critical boundary in the idea of the VLSI module. The rising velocity and intricacy of the present plans shows that a large number of procedures for diminishing VLSI chip energy are expanding significantly. Over the course of the past year, the ICs of 100million semiconductors have timed over 1GHz, in light of the fact that strength is thought about over terms of district and distance. The types of various flows that help the power dissemination have spillage present. The ongoing courses through parasite diodes created between channel mass and source mass districts, with a short channel impact prompted by a decrease in semiconductor scaling. The release is characterized into the dissemination of static power and the unique scattering of force. Static dissemination of the spillage power and the reserve force. The power dissemination of the short out because of the current is progressively scattered.

Drawbacks:

Power Optimization:

Various techniques used for testing, its application and disadvantages are shown in below

Table 1 Various techniques used for testing, its application and disadvantages

Technique	Disadvantages	Application
Test Vectors Reordering	For large set of test vectors, the CPU time needed to reorder vectors is bit high.	External Testing
Low Transition TPGs	Need a longer sequence of test vectors to get a high fault coverage.	Test-per-Scan BIST & Test-per-Clock
X-Filling	They require more test patterns to achieve a target fault coverage.	Test-per-Scan BIST
Scan Cells Reordering	Routing congestion problems during scan routing.	Test-per-Scan BIST
Test Vector Compaction	In some cases more test patterns are needed to get a target fault Coverage	Test-per-Scan BIST & Test-per-Clock
LFSR Parameter Selection	Needs huge CPU time to find the best parameters (e.g. the best seed).	Test-per-Scan BIST & Test-per-Clock
Low Power ATPG	Needs more CPU time than conventional ATPG	External Testing
Scan Architecture Modification	Hardware area overhead is significantly increased	Test-per-Scan BIST
LFSR Reseeding And Compression Techniques	Needs a moderate hardware area overhead	Test-per-Scan BIST

Power Estimation:

In power estimation, simulation and probabilistic methods are used. These methods require detailed structure of the circuit and its interconnection. There is a tradeoff between accuracy and efficiency. It requires more time to implement and simulate for large circuits.

VLSI Circuits:

PCs for processors, RAM, control module, and so on utilize installed modules. ICs frequently allude to exchanging components, informing stages, registering networks, vehicles, sound instruments, toys and body inserts. The innovation of the Micro-Electro - Mechanical System (MEMS) works with the development of interdisciplinary mechanical hardware on IC, consolidating limited scope mechanical and electronic frameworks. Sensors and speed increase capacity for auto airbags are, for instance, introduced on a chip where an accelerometer sense a quick expansion in the vehicle speed and distinguishes a looming crash. These improvements made the ICs for normal use and one of the best achievements of humankind.

In these most recent fifty years, the semiconductor count has developed from two or three hundred to in excess of 20 million. The semiconductors are five ages. Somewhat recently specifically, significant advances for electronic gadgets and cell phones have been noted in the IC business. This creates it impossible to miss in the approaching ten years that few Giga Hertz

can be utilized for chip working with a large number of semiconductors and that great many mechanical and electrical hardware can be utilized for Micro Electronic mechanical chip development. These chips will permit another period of cell phones that incorporates these applications as increased discernment, wearable and implantable PCs. It will give all individuals financially savvy, territorial highlight - point availability. The advancement of IC innovation started during the 1960s with the incorporation of not very many semiconductors (SMIS). A huge number of semiconductors consolidated into one chip are really being alluded to as VLSI (Very Large Scale Integration) chips. Present day ICs were more straightforward and given a couple of flip-failures and entryways. For a solitary semiconductor with a straightforward condenser organization, a few ICs were more comprehensible for carrying out an intelligent role."

Throughout the course of recent years, exceptionally huge point of interaction engineering has been developing tremendously with screen sizes diminished from the micrometer to the nanometer. The standard of Moore takes note of that each 1.5 years the combined semiconductors on a solitary incorporated circuit increment. The exchange scopes of a few hundred semiconductors for every circuit to the few large number of semiconductors each day per single chip. Exclusively by diminishing the component sizes of the incorporated circuit is this critical relocation conceivable. The down to earth sizes were changed from a couple of meters to a couple of nanometres. To accomplish high gadget effectiveness, electronic plan computerization (EDA), because of the developing trouble of present day VLSI chip configuration, assumes a critical part. The compositional arranging process for VLSI incorporates apportioning, floor planing, orchestrating, directing and compacting. The enormous expansion in VLSI circuits will in future rely on the progression of assets for actual framework computerization.

Review of Literature:

Arkadiy et al (2014) in 2002, it was recommended that the Gate Diffusion Input (GDI) procedure decrease the region and force of computerized VLSI circuits. For twin-well, silicone on Insulator (SOI) techniques, the GDI rationale was at first proposed. It permitted the execution with only two semiconductors of a large number of troublesome intelligent capabilities. This game plan was reasonable for the plan of customary computerized circuits which had a lot more modest region than existing PTL and Static CMOS strategies, while further developing power. Furthermore, GDI circuits were impacted by a diminished swing because of limit declines as were PTL executions. On the other hand, notwithstanding the requirement for swing reclamation circuits, the intelligent adaptability and semiconductor count of the GDI cell have diminished significantly.

T. Suguna and M. Janaki Rani (2018) "In light of the fact that the power

request is diminished, CMOS is the critical part in planning VLSI gadgets. Power streamlining in profound submicron CMOS advancements has turned into a superseded concern. As the PC is more modest, the key issues are power utilization cuts and in everyday power preservation on the processor. Power the executives is basic for some plans to diminish bundle expenses and draw out battery duration. The spillage of control the executives likewise plays a major part in the general power dissemination of VLSI circuits. This exposition tries to explain the progressions and advances in the space of force the executives in profound submicron districts of CMOS circuits. This overview was valuable for the originator to pick a suitable innovation as indicated by the prerequisite."

The creators in Tennakoon and Sechen (2012) recommended a compelling entryway estimating procedure for lagrangian unwinding with clear requirements. Be that as it may, the philosophy requires the down to earth harmonization of a decent introductory arrangement and subgradient streamlining. The creators in Berkelaar and Jess (2013) proposed an adaptable straight programming framework for entryway size in a bid to increment code refinement without significant impact on arrangement consistency. Furthermore, two well known techniques for further developing circuit execution are support addition and wiring with regards to expanding wire delay. The impediment of a net relies upon the wire obstruction and limit item straightforwardly."

Ambily Babu (2014) "Originators have been tracking down ways of accelerating computerized circuits and the their field of plan since the appearance of the First IC. Progresses in VLSI fabricating advancements as of late permitted the total Device to be mounted on a chip. The disadvantage was that the power dissemination of present day VLSI is a significant boundary. This paper gives understanding into explicit energy dissemination sources in computerized CMOS and the advancements for circuit and framework power streamlining."" Duan et al. (2009) Suggesting a procedure of transport encoding involving restricted cross-talk decrease momentary free calculation for onchip interconnection with the VLSI. A rendition of the parallel Fibonacci number technique was presented as planning and coding strategy. The numerical examination showed that the Fibonacci Numeral System (FSN) can address all numbers through Forbidden Transition Free (FTF) vectors which diminished the crosstalk delay and helped the methodology in which the free parallel Fibonacci coding words are produced.

M. Sivakumar and S. Omkumar (2017) Optimizations at various plan stage stages, like calculations, programming, rationale and circuit and cycle advancements, are expected to accomplish a decrease in power utilization. This paper checks out at the two rationale answers for programming engineering with low limit. For raising the exchanging activity limit of

individual rationale entryways, streamlining methodologies are performed. The power might be that by streamlining the circuit or limiting the intelligent stage. Inside this paper we seek after the technique for circuit level streamlining to each the district and strength. The proposed nonconcurrent equal self-time snake (PASTA) innovation utilizes adjusted Gate Diffusion Input (GDI) rationale. Similarly, the XOR entryway and half viper structure is diminished to a low surface and a low energy material. "The digialcircuit is fixated on the multi-esteem guideline by developing the portrayal space from the two rates (N=2) to N>2. The critical advantage of this technique is making up for the powerlessness to implement the uniform series of MVL entryways on current underlying circuits. The proposed Adder GDL rationale gives less semiconductors (region) and a low power utilization from the tests than the ongoing innovation. The proposed MVL innovation works with the development of a computerized MVL circuit bundle to get parallel circuit values. The reproduction stage is completed by the gadget tanner14.11 to test the unwavering quality of the PASTA and MVL circuits, while having little power and restricted wiring postpones comparative with parallel and three-esteem rationale.

Coello (2011) Emphasizes multi-objectif streamlining through transformative hypothesis and portrays the various methodologies using this methodology. The creator notes, for streamlining VLSI circuits by weighted summation that the extra objective capabilities might be utilized to produce a solitary component. Specifically, the creator exhibited in Vector Evaluated Genetic Search (GS), the adjusted adaptation of traditional GS during the determination step, the viability of some blend circuits and multiplier - free IIR channels. Kumar et al., (2010) have likewise examined a methodology to perceive in a completely determined set of vectors the don't mind areas, remembering both shortcoming enactment way and shortcoming proliferation way, which depends on PSO for vector reordering. Cell Automata (CA) is a strong registering and demonstrating device wherein the phone is refreshed at each clock cycle. The condition of the phone is directed by the prompt neighbors, ordinarily named as two states-three neighborhood CA. Utilization of CA has been accounted for in writing for testing of the VLSI circuits.

Semiconductor width, entryway scale, and link size issues are essential to VLSI engineering as they might permit decisions between the various needs of the expense highlight. In Fishburn and Dunlop (2015)," TILOS utilizes an iterative semiconductor estimating procedure in light of curved programming in view of the responsiveness of basic postponements to improve execution. The benefit of TILOS is that a neighborhood ideal is worldwide is the utilization of curved postpone models for semiconductor size. The iterative methodology has been additionally gotten to the next level. In any case, for issues of in excess of two or three

thousand expansive parts, the general methodology doesn't work.

Skobtsov et al. (2010) Two VLSI circuit TPG structures have been distinguished. One technique depends on the traditional GA, while another strategy incorporates hereditary programming, which shows the test designs as a miniature operation succession. For the representation of patterns and related processes, for example hybrid and change, a straight diagram portrayal is utilized. PSO is a strong stochastic multitude development and information streamlining methodology. PSO alludes to critical thinking the possibility of social contact. In this innovation, a bunch of particles which structure a multitude, moving around in the pursuit space, are viewed as a point in N-layered space that changes traveling to their own flying experience, alongside the flying experience of different particles.

Anuj and Divya Khanna (2014) Low power came in to spotlight in the ongoing age of electronic plan. Prior region and cost and execution were the need of configuration engineers disregarding power. Be that as it may, compromise exist between region, power and execution. The circuit is impacted by its parts in its general execution. Adding to plan issues and parts is finished to streamline the plan. The contracting innovation under 90 nm of force dissemination and its control was vital for the producer. Expanded battery duration and diminished bundles cost were fundamental for streamlining. This paper gives a writing survey on VLSI low-power circuit plan techniques and philosophies. The paper presumes that different energy decrease procedures and philosophies have been talked about. The CAD strategies for energy streamlining, which holds up with district and time and productivity have been successfully tried. This study showed that VLSI low power circuits are required and proposed various plan methodologies at present being used in the microelectronics business. This article permits originators to think about the essentials of low strength. The chief plan issues were in practically no time explained and acquainted with anybody who could get a kick out of the chance to find out about the subject."

Harutyunyan et al., (2012) examined another procedure for March test calculation age and its purposes in the RAMs for shortcoming identification. An original test calculation was produced for identification of all unlinked and connected static and two-activity dynamic deficiencies. In such manner, another construction situated technique was created and an efficient test calculation March LSD was produced. The writing shows that various specialists have taken care of business on March calculations. Further, it is seen that the vast majority of them have chipped away at the shortcoming inclusion and intricacy. Be that as it may, none of these papers reports the region above and power investigation of these calculations, as far as we could possibly know.

Sathiamoorthy and Andaljayalakshmi (2014) in fostering the connected areas for a scope of circuit modules on a chip, the idea of the actual design of VLSI circuits is a fundamental stage in expanding circuit yield. In this stage, it is typical for a producer to screen the area of specific modules for different purposes in the last bundling. The originator could decide to restrict the differentiation between two parts when there are different connections. It frequently happens as undertakings are utilized, in which the design remains something very similar with those parts in the ongoing floor plan. Creation firms may likewise be keen on a requirement that is balanced. Be that as it may, a compelling approach to observing the outright or relative area of modules isn't straightforward and, as a result of this shortcoming, the execution and convenience of many arrangement calculations have been restricted.

Lee and Touba, (2007) A new low power pressure information test gadget zeroed in on LFSR reseeding was likewise recommended. One disadvantage of LFSR-based pressure frameworks was that the unidentified pieces were stacked with obscure qualities, bringing about successive changes while examining and subsequently high dissemination. Another encoding framework was carried out to address this issue, which could be utilized for any LFSR reproduction technique, to diminish testing power emphatically and subsequently bring down the test limit. After LFSR reseeding, the proposed encoding framework was the second phase of pressure. Two objectives were reached: first and foremost, by filling the undefined pieces with a particular goal in mind how much changes was diminished; furthermore, by decreasing the quantity of characterized pieces to be produced by LFSR resetting. Exploratory work has shown that the proposed approach significantly brings down test power and offers preferable pressure of test information over LFSR reseeding alone proposes a lower-controlled streamlining calculation that has had the option to investigate the harmony between low power and high testability. A recently recommended power projection technique and a conjecture of the expected test time are utilized to quantify the calculation. The technique has been displayed for testability purposes through research facility control and field streamlining."

Ehrgott and Gandibleux (2012) Details of cutting edge MOP goal are portrayed, including Fuzzy methodologies, computerized strategies and formative calculations. Multi-target streamlining methodologies are utilized for the arrangement of simple and computerized circuits. Multilateral streamlining is a focal examination subject in science and designing. Various recordings, survey papers and even reading material on this subject are distributed. Different perspectives are characterized of non-straight multi-target streamlining.

Sellathamby et al., (2005) Suggested BIST low power yield. Advances are limited in their capability by developing the distance

between the accompanying pieces in the test arrangement, completed utilizing refreshed LFSR. The discoveries of the reproduction demonstrate that the power scattering with changed LFSR is that. Have sent off the most recent TPG with a diminished power dissemination that is more appropriate for BIST frameworks without influencing shortcoming cover. The examples produced by a counter and a dark code generator are XOR-ed with the low power seed LFSR. The outcome shows critical testing power decrease with the proposed technique. To test the VLSI Modules, LFSR is a significant piece of BIST to produce the examples for the testing. Numerous specialists have chipped away at the low power procedures for LFSRs and counters."

Van Ginneken (2010) introduced an ideal support inclusion calculation in light of dynamic programming. The quantity of cushion destinations that were the establishment for a few resulting concentrates on net support organization has a quadratic intricacy. On account of its varieties, it is accurately estimated by changing the processor voltage and fixing timing blunders. As opposed to more regrettable lodging and numerical streamlining, the Razor stage dispenses with the prerequisite for voltage edges and in this manner an enormous above economy."

Kapil Mangla and Shashank Saxena (2015) in day today life, Product Chip Systems (SoC) are required. The SoC is named as a large number of chips in a single opening. These million chips are incorporated into the single chip by diminishing each chip's semiconductor size. This CMOS procedure can consequently be utilized in the SoC item. CSLA is for the most part used to diminish the size of the chip and raising the hole of proliferation. The nonconcurrent programmed equal viper (PASTA) works by iterotic coding. Consequently, this snake eliminates the quantity of undesirable clock cycle initiation to accomplish high velocity and low power.

Lundstrom (2007) Rapid specialized development impacts designing advancement. The specialized progression permits imaginative and better PC gadgets to be delivered, in this manner advancing the development of a few development fields. The requirement for high precision and effectiveness is more noteworthy than any time in recent memory for multi-utilitarian tablets, cameras and workstations. Other than traditional effectiveness enhancements, clients are associated with battery duration, sturdiness and inexhaustible registering. Multi-utilitarian qualities, a superior presentation with low assets, conservative and simultaneously financially savvy are the fundamental targets of planning these merchandise. A typical technique to achieve these targets is the estimations of the essential components of the circuit. On account of developing spillage energy and sturdiness issues, the shift to bring down innovation ages for high effectiveness and denser application is getting more confounded. In this manner, the retrogressive movement

of creation moves toward the limits of ballistic vehicle."

Dennard et al (2018) the improvement in VLSI advancements has molded the simple and computerized circuits to downsize into nanometer range, the worry with respect to control utilization has expanded expediently because of the construction thickness and the plan entanglement. In this manner, there exists an essential of an exact power demonstrating procedure to coordinate the issues of nanometer handling advancements. In this paper a few demonstrating strategies have been examined and the course of Input Vector Control (IVC) is viewed as an ideal substitute in getting the low power utilization. IVC configuration is based on the impact of semiconductor stacking. It is incredibly liked due of its temperament of independency on the other innovative boundaries.

Gary Yeap (2008) we distinguished different spillage and static current decrease methodologies, voltage exchanging, capacitance, recurrence exchanging and saw an assortment of the normal low power engineering merits. The standards for low power engineering were portrayed by Sung-mo Kang et al, (2013), and various philosophies were proposed for low power utilization. The critical accentuation of this section was the circuit - or semiconductor engineering."

Geetha et al (2017) the critical test for late equipment organizations is low strength. Control scattering is a fundamental thought for VLSI Chip frame with regards to execution and region. Check the executives methodology are for the most part utilized for low power circuits and structures arrangement. Results show that the semiconductor spillage represents 40% or fundamentally higher total power usage. This rate would increase with the ascent in imagination on the off chance that legitimization methodologies don't add spillage inside regulation focuses. This paper centers around the improvement of circuits and plans motorization strategies to accomplish this point. The paper additionally frames different issues with the circuit limits at structure, legitimate and gadget rates and offers explicit ways to deal with resolve the previously mentioned issues. The underlying piece of the paper gives a timetable to essential wellsprings of CMOS semiconductor spillage current. The second segment of the paper uncovers a few methodologies for improving on the gadget to change the ongoing reserve spillage. A few current methodology, similar to rest, stacking and understanding procedures, are examined for CMOS entrance arranging that basically diminishes spillage streams. This paper talks about the advantages of the peruser approach since there is no additional observing and equipment assessment, consequently restricting the reach increment and furthermore, rather than other gadget, the power dissemination in unique state and not affecting the powerful limit that is the fundamental impediment of other spilling decrease strategies.

Conclusion and Future Work:

The disintegration techniques can be additionally summed up for not completely determined Boolean capabilities. This work anyway leaves various issues opens and issues to address giving a degree for additional expansion of this examination. The crude planning approach believed the entryways to be of "and", "or" qualities as it were. Further functionalities can be viewed as in the underlying planned circuit and new arrangement of rules can be determined in like manner for blend activities. Ideas like normal case postpone as far as not completely characterized Boolean capabilities and utilization of consistent exertion in assessing the deferral can likewise be utilized. Additionally, different methodologies for multi objective streamlining and picking of the best up-and-comer from the Pareto ideal front can be investigated. The clock gating rationale is streamlined involving our proposed approach with regards to exchanging power and region. Be that as it may, the gating rationale fundamentally influences the postponement of the circuit. Consequently execution boundary can likewise be remembered for the investigation.

References:

[1]. "Low power VLSI chip design: Circuit Design Techniques," http://www.eeherald. com/section/design-guide/Low-PowerVLSI-Design.html, accessed: 2014-12-25.

[2]. A. Peiravi and M. Asyaei, "Current-comparison-based Domino: New Low-leakage High-speed Domino Circuit for Wide Fan-in Gates," IEEE Transactions on Very Large Scale Integration Systems, vol. 21, no. 5, pp. 934–943, 2013

[3]. Ambily Babu (2014) "Power Optimization Techniques at Circuit and Device Level in Digital CMOS VLSI – A Review" International Journal of Engineering Research & Technology (IJERT) IJERT ISSN: 2278-0181 IJERTV3IS110434 www.ijert.org (This work is licensed under a Creative Commons Attribution 4.0 International License.) Vol. 3 Issue 11, November-2014

[4]. Anuj and Divya Khanna (2014) "A Literature Review on Design Strategies and Methodologies of Low Power VLSI Circuits" IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 4, Issue 2, Ver. IV (Mar-Apr. 2014), PP 17- 21 e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197 www.iosrjournals.org

[5]. Arkadiy Morgenshtein, Viacheslav Yuzhaninov, Alexey Kovshilovsky and Alexander Fish, "Full-Swing Gate Diffusion Input logic-Case-study of low-power CLA adder design", Integration, the VLSI journal, Vol. 47, 62-70, 2014.

[6]. B. R. Zeydel, D. Baran, and V. G. Oklobdzija, "Energy-efficient Design Methodologies: High-performance VLSI Adders," IEEE Journal of Solid-State Circuits, vol. 45, no. 6, pp. 1220–1233, 2010. [7] B. T. Geetha, B. Padmavathi and

V. Perumal (2017) "Design methodologies and circuit optimization techniques for low power CMOS VLSI design" DOI: 10.1109/ICPCSI.2017.8392016 https://ieeexplore.ieee.org/document/8392016

[7]. C. A. Coello, "A short tutorial on evolutionary multi objective optimization," in Proc. 1st Int. Conf. Evolutionary Multi Criterion Optimization, 2011, pp. 21–40

[8]. C. Efstathiou, Z. Owda, and Y. Tsiatouhas, "New High-Speed Multioutput Carry Look-Ahead Adders," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 60, no. 10, pp. 667–671, 2013.

[9]. Coello, Carlos A., Christiansen, Alan D. & Hernández Aguirre, "Using Genetic Algorithms to Design Combinational Logic Circuits." ANNIE'. Intelligent Engineering through Artificial Neural Networks, Volume 6. Smart Engineering Systems: Neural Networks, Fuzzy Logic and Evolutionary Programming. Edited by Cihan H. Dagli, MetinAkay, C. L. Philip Chen, Benito R. Fernandez and Joydeep Ghosh. pp. 391-396. November, 2016.

[10]. D. A. Patterson and J. L. Hennessy, Computer Organization and Design: The Hardware/Software Interface. Newnes, 2013.

[11]. Dennard RH, Cai J, Kumar A. A Perspective on today's scaling challenges and possible future directions: in Handbook of Thin Film Deposition (Fourth Edition).2018:3-18.

[12]. Duan, C., Calle, V.H.C. and Khatri, S.P. (2009), "Efficient on-chip crosstalk avoidance codec design", Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 17 No. 4, pp. 551-560.

[13]. F. J. Rodriguez, C. Garcia-Martinez, and M. Lozano, "Hybrid Meta-heuristics Based on Evolutionary Algorithms and Simulated Annealing: Taxonomy, Comparison, and Synergy Test," IEEE Transactions on Evolutionary Computation, vol. 16, no. 6, pp. 787–800, 2012

[14]. G. Martin, B. Bailey, and A. Piziali, ESL Design and Verification: A Prescription for Electronic System Level Methodology. Morgan Kaufmann, 2010.

[15]. G. Palumbo, M. Pennisi, and M. Alioto, "A Simple Circuit Approach to Reduce Delay Variations in Domino Logic Gates," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, no. 10, pp. 2292–2300, 2012.