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An Examination Of The Design Challenges Faced During SOC Design

Ms. Neha Bhutada[1] & Dr. Archana Tukaram Bhise[2]
[1]*Ph.D. Research Scholar, Department of Computer Science, Shri. JJT University, Rajasthan, India.*
[2]*Professor & Research Guide, Department of Computer Science, Shri. JJT University, Rajasthan, India.*
Corresponding Author - Ms. Neha Bhutada
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Abstract:

The integrated circuit industry started using a new design process known as System on Chip (SOC) Design over the course of several years, during which time the complexity and cost of integrated circuits continued to rise as the geometry continued to shrink at an exponential pace. A system-on-a-chip, or SOC, is essentially an integrated circuit that integrates all of a system's components onto a single chip. They are manufactured with a wide variety of cores in the production process. Various design difficulties emerge as a consequence of the use of these various kinds of cores in conjunction with the growing complexity of integration, interfacing, and other verification tests at various levels of integration. In this research, an investigation of the design challenges faced during the creation of SOCs is presented.

Key words: SOC, Cores, IP

Introduction:

The semiconductor industry has made remarkable strides in recent years in increasing the density of very large-scale integrated (VLSI) circuits [1]. Design engineers have created new processes and procedures in order to handle the growing complexity that is inherent in these huge chips. This is done so that they can stay up with the degrees of integration that are now accessible. The design of system-on-chip (also known as SoC) is one example of an evolving technique. In order for a SOC to be created such that it can give complete functionality for an application on an IC, distinct numerous stand alone VLSI designs need to be stitched together throughout the design process. They can be designed utilising an ASIC vendor design, in which case all of the components are produced by a single vendor; an integrated design, in which case some components are produced by the vendor, while others are obtained from other sources; or a desktop design, in which case all of the components are pieced together from various sources by a fables company [2,8]. These design methods are applicable to the design of SOCs, and they are quite successful.

The integration of additional devices into the system makes the design of the system more difficult and complicated. Despite the fact that the size is becoming smaller, it is important to remember crucial design considerations such as power consumption, LVS (Layout vs. Schematic), DRC (Design Rules Check), timing difficulties, design validation, and so on. In order to make the most of the new design technology, these factors need to be tuned. As a result of this mismatch, there are several design issues that develop. Issues like as power efficiency, design for test, and latency are included in this category. One such approach is design re-use. It is possible to repurpose the existing cores or intellectual property (IP) in order to save time and money while yet satisfying the demand in a timely way. The building blocks for new SOCs come from the designs of the SOCs that came before them. Embedded processors, memory blocks, interface blocks, analogue blocks, and components that manage application-specific processing operations are all examples of the types of reusable IP cores that may be included in these IP cores [3,4].

Design Issues:

Power Consumption:

It is challenging to deliver power to the growing number of integrated transistors on a single chip because of the limited space available. As a result, the system need to have great performance while using a minimal amount of electricity. This highlights the need of developing low-power systems, since the amount of power used is a crucial criterion. Because the rate at which power dissipation per transistor is decreasing is not keeping pace with the rate at which gate density is rising, the power density of future SoCs is expected to rise. Because of this, we need to decrease the total power consumption of the system by using the design of the system architecture rather of depending just on process technology [5].

Latency:

The memory wall refers to the ever-widening performance gap that may be seen between the speeds of the CPU and the memory. [4] Embedded memory are being included into the same chip as other components by the designers so that they may address this issue. In addition, as the number of components increases, it becomes much more challenging to provide the exact identical clock signals to each individual component at the same time. As we get farther along in the process of timing analysis and verification for the SOC, this becomes a significant problem with the design.

Design for Verification:

One of the steps in the chip design flow that takes up the most time is the design for verification and for testing stage. Even a relatively little alteration to the circuit will force the designer to reevaluate the overall performance of the device as well as recheck the timing analysis of the circuit. The time required to validate a design increases when one billion components are packed onto a single chip. The co-development technique, also known as the use of both hardware and software design, is beneficial in that it helps reduce the amount of time spent on verification and testing. In addition, while creating SOCs, it is common practise to combine intellectual property (IP) components sourced from a variety of suppliers into a single platform. As a result, there is a pressing need to develop a comprehensive and efficient design approach for SOC.

Reconfigurable Logic:

Since quite some time ago, designers have been incorporating field-programmable gate arrays (FPGA) into board-level designs. Some architectural designs begin to include logic operations and interconnects that are capable of being altered while the system is running in order to facilitate the production of high-performance, flexible platforms. The freedom to change the functionality of the SOC after manufacturing is provided by the addition of reconfigurable logic to the SOC. These designs have the ability to deliver improved performance and power economy while providing more flexibility as compared to programmable CPUs.

Static Timing Analysis:

Because of the presence of numerous voltages, libraries may not be described at the precise voltage that we are using, which makes timing analysis far more difficult. The conclusion is that the design need to be capable of satisfying the temporal and power requirements for each and every mode and corner circumstance. Designers have the responsibility of ensuring that the appropriate level shifters, retention cells, and other design features have been precisely positioned for each of the various power domains. Additionally, they must verify that bulk and well connections have been made at the transistor level. These inspections may be automated with the use of tools developed by EDA companies [6].

Other Design Issues:

As was noted before, today's designers are increasingly turning to embedded memories that are incorporated on the same chip as the rest of the system. This makes it simpler to synchronise the memories with the system and removes the need for any additional hardware. There

are several obstacles to overcome when attempting to strike a balance between power and efficiency. SRAM offers excellent performance, however flash memory is the most efficient option in terms of the amount of power it consumes. [4] In a similar fashion, many processors are also combined on the same chip, and we may boost the efficiency of the SOC by using a technique called parallel pipelining. When utilising an approach that allows for portability, a few extra design challenges might emerge. Examples include step sizes that rely on the arrangement, mismatches in aspect ratio, and core that is not netlisted. Problems with timing include clock redistribution, discrepancies in hard core width and spacing, differences in antenna rules, RC parasitic owing to chip layers, timing reverification, and circuit timing.

A variety of associations that have been formed to give recommendations for the design of cores and how to utilise them may provide a solution to these challenges, which can then be resolved. The Pinnacles Component Information Standards (PCIS) programme was developed by the Reusable Application-Specific Intellectual Property Developers (RAPID) organisation. The Electronic Component Information Exchange (ECIX) programme was developed by the Silicon Integration Initiative (Si2) organisation. The Embedded core design and test specifications were developed by the Virtual socket Interface (VSI) Alliance.

Conclusion:

SOCs are becoming more advanced in terms of their capabilities as VLSI technology continues to advance. These SOCs have a significant number of clock and power components, in addition to a huge number of IPs and memory. These kinds of multi-power domain SOCs are complicated and present new integration challenges due to the fact that many blocks have different operating modes at different voltages, different clock periods, and different duty cycles for each block depending on whether it is awake, asleep, or in the shutdown mode. We need to pay greater attention to the applications that govern the modes of operation, the required amount of power, and the minimum battery life [7]. The architecture of the SoC needs to take into account the overall system's performance, flexibility, and scalability, as well as power and thermal management, system partitioning (digital, analogue, on-chip, or off-chip), architecture partitioning (hardware and software), algorithm development for new applications, and so on. [4] Although power gating and other strategies are useful in today's world, it's possible that these methods won't be adequate for many

low-power SOCs used in IoT devices. We are required to consider in terms of design-for- power in terms of energy consumptions at all stages of design, including overall system/application, architectural, power management, RTL, DFT, and physical implementation, in addition to technological and process improvements [7].

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